REMARKS

In the Office Action, the Examiner rejected claims 28-31, 34-36, 39-46, 49-51, and 54-57 under § 102 as being anticipated by USP 5,822,214 issued to Rostoker et al. (Rostoker). The Examiner rejected claims 32, 33, 37, 38, 47, 48, 52, and 53 for their dependence upon a rejected base claim. However, the Examiner found claims 32, 33, 37, 38, 47, 48, 52, and 53 otherwise allowable. The Examiner also found claims 58-75 allowable. In this Amendment, Applicants have amended claims 28, 34-36, 38-43, 49, 50, 51, and 53-57. No claims have been added or canceled. Accordingly, claims 28-75 will be pending after entry of this Proposed Amendment.

I. Interview

Applicants respectfully thank the Examiner for the personal interview on August 16, 2004. During the personal interview, no exhibit was shown or demonstration conducted. Applicants' representative discussed the independent claims and the cited references with the Examiner. Pursuant to the discussion in the interview, Applicants have amended independent claims 28, 37, and 43 in this Amendment. In addition, Applicants have amended the dependent claims 34-36, 38-42, 49, 50, 51, and 53-57 to harmonize with these amended base claims.

II. Informalities in Claim 38 and 53

The Examiner objected to claims 38 and 53 because the phrase "said slots" lacked antecedent basis. Applicants have amended claims 38 and 53 to replace the phrase "said slots" with the phrase "said sub-regions". Applicants respectfully submit that claims 37 and 52 provide antecedent basis for the phrase "said sub-regions".

III. Rejection to Claims 28-31, 34-36, and 39-42

The Examiner rejected claims 28-31, 34-36, and 39-42 under § 102 as being anticipated by Rostoker.

Claims 29-31, 34-36, and 39-42 are dependent directly or indirectly on independent claim 28. Claim 28 recites a method of placing circuit elements in a region of an integrated circuit ("IC") layout. Several nets represent interconnections between the circuit elements. Each net is defined to include a set of circuit elements. This method partitions the IC region into several sub-regions, where several edges exist between the sub-regions. Several of the edges are diagonal. The method selects a net and identifies the set of sub-regions containing the circuit elements of the selected net. The method identifies the edges, from the several edges, intersected by at least one set of interconnect lines necessary for connecting the identified set of sub-regions. At least one of the identified edges is diagonal. The method computes a placement cost for the net by using the identified edges.

Applicants respectfully submit that Rostoker does not disclose, teach, or even suggest such a method. The Examiner identifies column 42, lines 48-58 and column 56, line 56 to column 59, line 63 of Rostoker as disclosing the identification of edges intersected by at least one set of interconnect lines necessary for connecting an identified set of sub-regions limitation of claim 28. However, as characterized by the Examiner, these passages of Rostoker disclose a "Steiner tree" implemented during a routing operation. This routing operation as disclosed in Rostoker transpires after a placement operation. Moreover, Rostoker does not mention a set of interconnect lines necessary for connecting an identified set of sub-regions in the sections where Rostoker discloses its placement operation. Therefore, Rostoker does not disclose, teach, or even suggest the recited method of claim 28 that places circuit elements in a region of an integrated circuit ("IC") layout by identifying edges intersected by at least one set of interconnect lines necessary for connecting an identified set of sub-regions, and computes a placement cost for the net by using the identified edges.

The Examiner identifies column 59, lines 41-62 of Rostoker as disclosing the computation of a placement cost for a net by using the identified edges limitation of claim 28. However, this passage of Rostoker discloses computing costs during a routing operation. Moreover, Rostoker does not mention computing costs in the sections where Rostoker discloses its placement operation. Therefore, Rostoker does not disclose, teach, or even suggest the recited method of claim 28, which computes a placement cost for a net by using the identified edges.

Accordingly, Applicants respectfully submit that Rostoker does not render claim 28 unpatentable. As claims 29-31, 34-36, and 39-42 are dependent on claim 28, Applicants respectfully submit that claims 29-31, 34-36, and 39-42 are patentable over Rostoker for at least the same reasons as claim 28. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the § 102 rejection of claims 28-31, 34-36, and 39-42.

IV. Claims 43-46, 49-51, 54-57

The Examiner rejected claims 43-46, 49-51, and 54-57 under § 102 as being anticipated by Rostoker.

Claims 44-46, 49-51, and 54-57 are dependent directly or indirectly on independent claim 43. Claim 43 recites a method of placing circuit elements in a region of an integrated circuit ("IC") layout. Several nets represent interconnections between the circuit elements. Each net is defined to include a set of circuit elements. This method partitions the IC region into several sub-regions, where several line paths exist between the sub-regions. Several of the line paths are diagonal. The method selects a net and identifies the set of sub-regions containing the circuit elements of the selected net. The method identifies several line paths used by at least one set of interconnect lines necessary for connecting the identified set of sub-regions. At least one of the identified line paths is diagonal. The method computes a placement cost for the net by using the identified line paths.

Applicants respectfully submit that Rostoker does not disclose, teach, or even suggest such a method. The Examiner identifies column 42, lines 48-58 and column 56, line 56 to column 59, line 63 of Rostoker as disclosing the identification of edges intersected by at least one set of interconnect lines necessary for connecting an identified set of sub-regions limitation of claim 43. However, as characterized by the Examiner, these passages of Rostoker disclose a "Steiner tree" implemented during a routing operation. This routing operation as disclosed in Rostoker transpires after a placement operation. Moreover, Rostoker does not mention a set of interconnect lines necessary for connecting an identified set of sub-regions in the sections where Rostoker discloses its placement operation. Therefore, Rostoker does not disclose, teach, or even suggest the recited method of claim 43 that places circuit elements in a region of an integrated circuit ("IC") layout by identifying edges intersected by at least one set of interconnect lines necessary for connecting an identified set of sub-regions, and computes a placement cost for the net by using the identified edges.

The Examiner identifies column 59, lines 41-62 of Rostoker as disclosing the computation of a placement cost for a net by using the identified line paths limitation of claim 43. However, this passage of Rostoker discloses computing costs during a routing operation. Moreover, Rostoker does not even mention computing costs in the sections where Rostoker discloses its placement operation. Therefore, Rostoker does not disclose, teach, or even suggest the recited method of claim 43, which computes a placement cost for a net by using the identified line paths.

Accordingly, Applicants respectfully submit that Rostoker does not render claim 43 unpatentable. As claims 44-46, 49-51, 54-57 are dependent on claim 43, Applicants respectfully submit that claims 44-46, 49-51, 54-57 are patentable over Rostoker for at least the same

reasons as claim 43. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the § 102 rejection of claims 43-46, 49-51, and 54-57.

V. Allowable Claims

In the Office Action, the Examiner found that claims 32, 33, 37, 38, 47, 48, 52, and 53 contain allowable subject matter, but objected to these claims as being dependent upon a rejected base claim. The Examiner also found claims 58-75 allowable. The Applicants thank the Examiner for these findings of allowability. Applicants have not rewritten claims 32, 33, 37, 38, 47, 48, 52, and 53 in independent form as their intervening base claims are believed to be allowable as discussed above.

CONCLUSION

In view of the foregoing, it is submitted that all pending claims, namely claims 28-75, are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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